MAINTENANCE HANDBOOK

MODEL 225
MODEM TEST SET

MP MASTER
MA28867

SYSTRON-DONNER CORPORATION
DATAPULSE

10150 W. Jefferson Blvd., Culver City, Calif. 90230
Tel: (213) 836-6100; TWX: 910-340-6766; Telex: 67-3219

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1.0 WIRING MODEL 225 FOR 115 V 60 Hz OR 230 V 50 Hz

The Model 225 may be wired to operate from either 115 V 60 Hz or 230 V 50 Hz power input.

The transformer schematic is shown in Figure 1 below. The primary terminals are marked 1, 2, 3 and 4.

For 115 V 60 Hz Operation:

(1) Connect terminal 1 to 3.

(2) Connect terminal 2 to 4.

(3) Connect the white power lead that comes from the fuse to terminal 2.

(4) Connect the blue power lead to terminal 1.

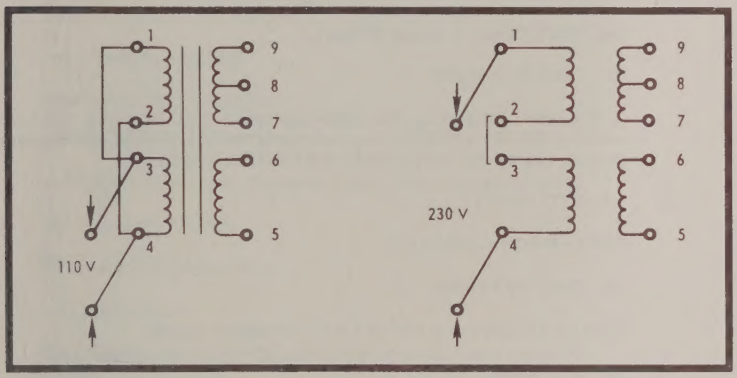


FIGURE 1. MODEL 225 TRANSFORMER SCHEMATIC

For 230 V 50 Hz Operation:

(1) Connect terminal 2 to 3.

(2) Connect the blue power lead to terminal 1.

(3) Connect the white power lead that comes from the fuse to terminal 4.

The Model 225 is normally wired for 115 V 60 Hz operation at the factory, and the power socket on the back panel is labeled 115 V 60 Hz.

For customers wishing to rewire the unit for 230 V 50 Hz operation, a small tag reading 230 V 50 Hz is supplied to facilitate relabeling the power socket with the new power constraint. The label adhesive may be activated by brushing on trichlorethylene solvent. An acceptable solvent is manufactured by Metal-Craft, Inc., Mason City, Iowa.

2.0 CALIBRATION PROCEDURE FOR MODEL 225 MODEM TEST SET

The following describes a procedure for calibrating the Model 225 Modem Test Set. It is assumed that the test set is not connected to any modem during this procedure.

1. (a) SETTINGS

   Set POWER switch to OFF. Set INVERT DATA/NORMAL switch to NORMAL. Set RECEIVE ONLY/TRANSMIT RECEIVE switch to TRANSMIT RECEIVE position. Set XMIT ERROR switch to OFF. Set TEST OPERATE switch to OPERATE. Set BIT ERROR/BLOCK ERROR switch to BLOCK ERROR. Set PATTERN switch to pattern length of 2047 bits. Set DATA RATE switch to 2400. Turn power ON.

   (b) OBSERVATIONS

   Bias meter to space condition. Clock Monitor light on. Error count is 000.

2. (a) SETTINGS

   Set TEST OPERATE switch to TEST.

   (b) OBSERVATIONS

   Sync locked light goes on. Bias meter oscillates pseudo-randomly about center position. NOTE: If NIXIES show errors and the SYNC RECOVERED lamp goes on, depress the SYNC RECOVERED RESET pushbutton.

3. (a) SETTINGS

   XMIT ERROR switch to ON.

   (b) OBSERVATIONS

   Error count increases at rate of 1 error per pattern length.

4. (a) SETTINGS

   BIT ERROR/BLOCK ERROR switch to BLOCK ERROR.

   (b) OBSERVATIONS

   Error count increases at rate of 1 error per pattern length.

5. (a) SETTINGS

   XMIT ERROR switch OFF. BIT ERROR/BLOCK ERROR switch to BIT ERROR. Depress and hold BREAK SYNC pushbutton.

   (b) OBSERVATIONS

   CLOCK MONITOR light goes off.

6. (a) SETTINGS

   Release BREAK SYNC pushbutton.

   (b) OBSERVATIONS

   NIXIES record large number of errors. OVERRANGE lamp lights. SYNC RECOVERED lamp goes on. ERROR COUNT resets to 000.

7. (a) SETTINGS

Repeat 1a through 6a with PATTERN switch set to 511 bit pattern length.

(b) OBSERVATIONS

Identical to 1b through 6b.

8. (a) SETTINGS

Repeat paragraphs 1a through 6a with PATTERN switch set to 63 bit pattern length.

(b) OBSERVATIONS

Repeat paragraphs 1b through 6b.

9. (a) SETTINGS

Repeat 1a through 8a at each data rate. (The EXT DATA RATE position will be covered in Section 16.)

(b) OBSERVATIONS

Identical to 1b through 8b.

10. (a) SETTINGS

PATTERN switch in ALT position at any data rate except EXT.

(b) OBSERVATIONS

Bias meter oscillates about 0.

11. (a) SETTINGS

PATTERN switch in MARK position at any data rate except EXT.

(b) OBSERVATIONS

Bias meter reads M.

12. (a) SETTINGS

PATTERN switch in SPACE position at any data rate except EXT.

(b) OBSERVATIONS

Bias meter reads S.

13. (a) SETTINGS

Repeat paragraphs 1 and 2.

(b) OBSERVATIONS

Repeat paragraphs 1 and 2.

14. (a) SETTINGS

Depress and release RESET COUNT pushbutton. Allow time for at least one pattern to be analyzed, then depress and hold the DISPLAY BLOCK COUNT pushbutton.

(b) OBSERVATIONS

A three digit number greater than zero is displayed. The OVERRANGE lamp will also be illuminated if 1000 or more patterns have been analyzed.

15. (a) SETTINGS

Release DISPLAY BLOCK COUNT pushbutton.

(b) OBSERVATIONS

ERROR COUNT reads 000.

16. (a) SETTINGS

Set POWER switch to OFF. Set INVERT DATA/NORMAL switch to NORMAL position. Set RECEIVE ONLY/TRANSMIT RECEIVE switch to TRANSMIT RECEIVE position. Set XMIT ERROR switch to OFF. Set TEST/OPERATE switch to OPERATE. Set BIT ERROR/BLOCK ERROR switch to BIT ERROR. Set PATTERN switch to pattern length of 2047 bits. Set DATA RATE switch to EXTERNAL. Apply 2400 b/s square wave to pin 15 and 17 of data connector. Apply signal ground to pin 7 of data connector. The MAXIMUM allowable voltage and current excursions for the input square wave are listed below for each interface circuit.

WARNING: DO NOT EXCEED VALUES LISTED.

EIA: -25 V to +25 V.

DTL/TTL: 0 V to 5 V.

MIL 188B: -6 V to 6 V.

CURRENT: 0 mA to 40 mA.

The MINIMUM allowable voltage and current excursions for the input square wave are listed below for each interface circuit.

EIA: -25 V to 2 V.

DTL/TTL: 0 V to 1.2 V.

MIL 188B: -0.6 V to 0.6 V.

CURRENT: 5 mA to 23 mA.

Vary amplitude of input square wave over above ranges specified for interface circuits installed in test set. Connect pins 2 and 3 together on back panel data connector. Turn POWER switch ON. Set the XMIT ERROR switch to the XMIT ERROR position.

(b) OBSERVATIONS

Sync locked light goes on. Bias meter oscillates in a pseudo-random manner about the center position. (NOTE: If NIXIES show errors prior to resetting to 000, the SYNC RECOVERED lamp will go on. Extinguish this lamp by depressing the SYNC RECOVERED RESET pushbutton.). Errors are detected at the rate of 1 error per pattern while XMIT ERROR switch is in the XMIT ERROR position.

The Model 225 with data synchronizing option allows the receiver section of the Model 225 to operate at asynchronous speeds other than those available by selection of the front panel. A slide switch and four BNC connectors are provided in the back of the unit for this purpose. All interface levels for the BNC connectors are standard DTL/TTL logic. The function of each of the input signals is described below.

3.1.1 DATA IN

This connector allows the input data to drive the receiver portion of the Model 225.

3.1.2 48 X RATE (REF)

This connector allows the external clock to drive the clock recovery system in the Model 225. The clock does not need to be phased with the data presented at the DATA IN input, but it must be within 2% of the DATA IN data rate.

3.1.3 DATA OUT

This connector allows the output data of the transmitter portion of the Model 225 to drive external equipment. This data is synchronized with the CLOCK OUT output.

3.1.4 CLOCK OUT

This connector allows the synchronized output clock to clock the DATA OUT to external equipment.

3.1.5 FRONT PANEL–OTHER

This is a slide switch which when in front panel position allows the Model 225 to operate with its own, front panel selected, data rates. When in other position, it operates as a data synchronizing terminal at any data rate dictated by the DATA IN and 48 X RATE reference clock.

3.2 SIGNAL MONITORING OPTION

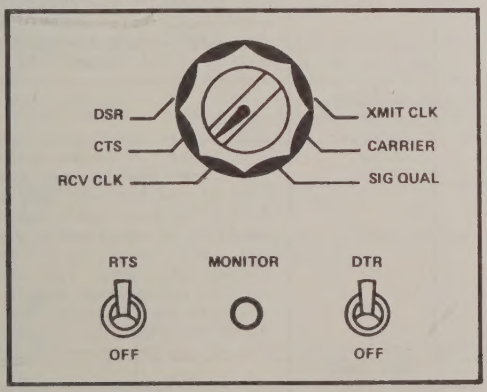


FIGURE 2. SIGNAL MONITOR OPTION

The purpose of this option is to allow certain key signals at the EIA interface to be controlled and monitored. A six-position rotary switch, mounted on a concentric shaft along with the pattern selection switch, allows the selection and monitoring of any one of six lines. In addition, two toggle switches allow control of the REQUEST TO SEND and DATA TERMINAL READY lines. These lines and their associated EIA pin assignments are given in Table 1 below.

In order to monitor the status of any of the above signals, select the desired signal with the topmost (red) knob on the MONITOR rotary switch. If the status of the selected line is "on", then the monitor light directly beneath the monitor rotary switch will be illuminated. Conversely, the light will remain extinguished for all "off" conditions.

DATA CONNECTOR PIN ASSIGNMENTS

PIN	IN/OUT	FUNCTION	DESCRIPTION
1	-	Chassis Ground	Tied to frame of Test Set which is in turn grounded to the power system ground through the power cord.
2	Output	Transmitted Data	A re-cycling pseudo-random binary sequence. Plus 12V = Logic "O"; minus 12V = Logic "1".
3	Input	Received Data	Received digital data, non-return-to zero. Plus 3 V to plus 25 V = Logic "O"; minus 3 V to minus 25 V = Logic "1".
4	Output	Request to Send	Plus 12 V level to indicate Test Set is supplying data for transmission.
5/6	--	Not Used	
7	--	Signal Ground	Provides reference point for all signals. In Test Set it is tied to frame.
8/14	--	Not Used	
15	Input	Transmitter Clock	Required in synchronous applications only. A square wave bit rate clock used to time the transmitted data. Plus 3V to plus 25V= Logic "O"; Minus 3V to minus 25V= Logic "1".
			Bit changes in the transmitted data signal will occur only in coincidence with a positive transition of the Transmitter Clock.
16	--	Not Used	
17	Input	Receiver Clock	Required in synchronous applications only. A square wave bit rate clock used to time the sampling of the Received Data Signal. Plus 3V to plus 25V = Logic "O"; Minus 3V to minus 25V = Logic "1". Bit changes in the Received Data signal must occur only in coincidence with a positive transition of the Receiver Clock.
18/19	--	Not Used	
20	Output	Data Terminal Ready	Plus 12V level to indicate Test Set is in a data transmission mode.
21/25	--	Not Used	

TABLE 2 - OPTION CONNECTOR SIGNALS
All output signals are +5V or 0V unless otherwise indicated

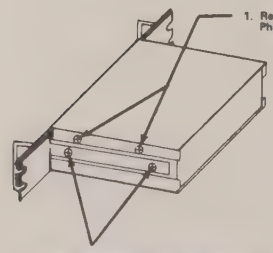
PIN #	SIGNAL	DESCRIPTION
15	1 Unit	BCD Error Counter Readout (0 volts = "One")
14	2 Units	"
12	4 Units	"
13	8 Units	"
10	1 Ten	"
11	2 Tens	"
8	4 Tens	"
9	8 Tens	"
6	1 Hundred	"
7	2 Hundred	"
5	4 Hundred	"
4	8 Hundred	"
17	Reset Error Counter	An external negative pulse resets Error Counter to zero and clears overflow indicator.
24	Receiver in Sync	Signal is 0 volts when receiver is in sync, +5 volts when out of sync.
19	Sync Recovered	Zero level indicates sync has been recovered.
16	Transmitter Clock	Data from Modem at transmitter.
22	Receiver Clock	Modem clock if synchronous, recovered clock if asynchronous. For bit sync purposes.
1	Start of Trans Period	Periodic pulse appearing at the beginning of each pseudo-random pattern transmitted.
23	Start of Receiver Period	Periodic pulse appearing in phase with the beginning of each pseudo-random pattern received.
3	Clock Monitor	Positive level indicates clock is present at receiver.
2	Error Pulse	A negative pulse appears each time an error is detected in received sequence.
18	Transmitter Data	Transmitted pseudo-random sequence ($\pm$12 volts).
20	Received Data	Received pseudo-random sequence ($\pm$12 volts).
21	Signal Ground	
25	Chassis Ground	

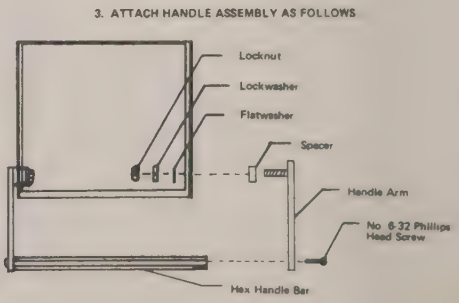
Note that the RECEIVED DATA line (pin 3, RS232B or C, designation "BB") is continually monitored by the TEST SET BIAS meter. The TRANSMITTED DATA (pin 2, RS232B or C, designation "BA") is not monitored but can easily be checked by putting the test set into the TEST condition thus tieing the TRANSMITTED DATA into the RECEIVED DATA and observing the BIAS meter.

DATA CONNECTOR PIN NUMBER.	RS232B or C DESIGNATION	FRONT PANEL LABEL	DESCRIPTION
6	CC	DSR	Data Set Ready
5	CB	CTS	Clear to Send
17	DD	RCV CLK	Receiver Signal Element Timing.
15	DB	XMT CLK	Transmitted Signal Element Timing.
8	CF	CARRIER	Receive Line Signal (Data Carrier) Detector.
21	CG	SIG QUAL	Signal Quality Detector.
4	CA	RTS	Request To Send.
20	CD	DTR	Data Terminal Ready.

3.3 RACK MOUNTING OPTION

Instructions for converting a rack mount to a table top model with handles are given below.


1. Remove top cover by removing two No. 4-40 Phillips head screws located on each side of unit.
2. Remove rack mount brackets by removing two No. 8-32 Phillips head screws on each bracket.



All of the DATAPULSE test sets utilize an eleven stage shift register which is capable of repetitively producing a PR word or block which is $2^{11}-1$ or 2,047 bits in length and contains all 2,048 possible combinations of 11 bits except eleven consecutive 0's. A simplified block diagram of the transmitter section is shown in Figure 5F below.

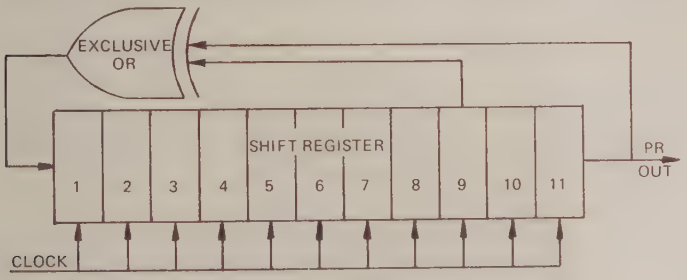


FIGURE 5F. PR GENERATION, TRANSMITTER SECTION

Note that this is exactly the same circuit as that which we studied in Figure 5C above, except that this shift register contains 11 stages for producing 2,047 bit words. Note that the feedback points are stages 11 and 9. These are determined mathematically to be the proper feedback stages to produce the maximal length (2,047 bit) word.

4.2 THE RECEIVER SECTION

The receiver section of your modem test set contains a shift register/exclusive OR PR generator that is identical to that found in the transmitter section. In addition, it contains circuitry for synchronizing the data generated in this second generator with the data being received from the system under test. It contains clock correction circuitry to insure that the clock used in the receiver PR generator is synchronized with that of the received data. It contains error detection circuitry. It contains circuitry to count and display bit or block errors and total blocks generated. And, finally, it contains circuitry for measurement and adjustment of bias distortion. Let us study these important features of the receiver section.

4.2.1 PR Regeneration and Error Detection

In the transmitter section described above, we generated a repetitive 2,047 PR data pattern to be transmitted into a system to be tested. That pattern is put through the system being tested and is taken from that system's output into the input of the receiver section of the test set. At this point we will generate a second 2,047 bit PR data pattern which is identical to the one we produced in the transmitter section. We will then compare the data from this second generator with the data which has come through the system being tested. If there are differences in the two data streams, we will know that the system under test has caused errors in the first data stream we generated. Figure 5G below is a block diagram of the receiver section PR generator and error detection circuits. Note that when the DATA SYNC switch is in position A, the incoming data will be loaded directly into the eleven-stage shift register. When the switch is in position B, the input to the shift register is disconnected from the incoming data and connected to the output of the exclusive OR feedback.

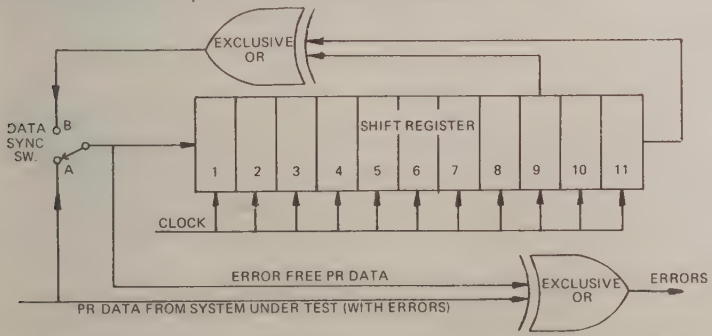


FIGURE 5G. RECEIVER SECTION—PR GENERATION and ERROR DETECTION

3.5 BLOCK LENGTH SELECTOR OPTION

This option provides the modem test set with a comprehensive block analysis capability. Figure 4 below illustrates the front panel switches and indicators that are provided with this option.

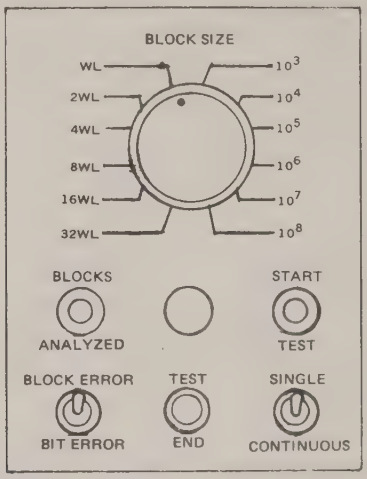


FIGURE 4. BLOCK LENGTH SELECTION OPTION—FRONT PANEL

Block sizes from 10^3 through 10^8 bits in multiple powers of 10 and 1, 2, 4, 8, 16 and 32 times the word (pattern) length (WL) in bits are selectable by a front panel rotary switch labeled BLOCK SIZE. A BLOCK ERROR/BIT ERROR toggle switch determines whether bits in error or blocks in error will be detected, counted and displayed. An internal counter continually tallies the number of blocks analyzed according to the setting of the BLOCK SIZE rotary switch, independent of the BLOCK ERROR/BIT ERROR switch position. At any time, the total number of blocks analyzed can be displayed simply by depressing a pushbutton labeled BLOCKS ANALYZED.

Blocks of data can be analyzed either one at a time or continuously depending on the position of a toggle switch labeled SINGLE/CONTINUOUS. In the SINGLE position, a single block of data, its size selected by the BLOCK SIZE rotary switch, is analyzed for errors on a bit-by-bit basis. The operator starts the test by depressing a START TEST pushbutton and the test automatically ends when the block of data has been completely analyzed for errors. An END TEST lamp lights to indicate this fact to the operator and the total number of errors in that block is displayed by the nixie display. Thus, the operator can determine the bit error rate directly by reading the nixie display and the setting of the BLOCK SIZE rotary switch. The test can be repeated simply by again depressing the START TEST pushbutton.

The block error rate can be determined directly by selecting the block size through the BLOCK SIZE rotary switch, setting the SINGLE/CONTINUOUS switch to CONTINUOUS and the BLOCK ERROR BIT ERROR switch to BLOCK ERROR. The nixies will display the running total of blocks in error while the internal block counter will tally the total number of blocks analyzed. This latter total can be displayed at any time by depressing the BLOCKS ANALYZED pushbutton. The analysis is halted while this pushbutton is depressed and continued when it is released.

The following controls and indicators are associated with this option.

3.5.1 BLOCK SIZE

DATA BLOCK sizes from 10^3 through 10^8 bits in multiple powers of 10 and 1, 2, 4, 8, 16 and 32 times the word (pattern) length (WL) in bits are selectable for analysis by this eight-position rotary switch.

3.5.2 SINGLE/CONTINUOUS

Blocks of data can be analyzed either one at a time or continuously, depending on the position of this switch. In the SINGLE position, a single block of data, its size determined by the setting of the BLOCK SIZE rotary switch, is analyzed for errors on a bit-by-bit basis. The analysis starts when the START/TEST pushbutton is depressed and ends when the block of data has been completely analyzed.

When this switch is in the CONTINUOUS position, data is continually analyzed either bit-by-bit or block-by-block, depending on the setting of the BLOCK ERROR/BIT ERROR switch.

3.5.3 START/TEST

This pushbutton is active only when the SINGLE/CONTINUOUS switch is in the SINGLE position. Depressing this pushbutton starts the analysis of a single block of data on a bit-by-bit basis.

3.5.4 END/TEST

Indicates when the analysis of a single block of data has been completed. This lamp operates only then the SINGLE/CONTINUOUS switch is in the SINGLE position.

3.6 POSITIVE NEUTRAL/POLAR/NEGATIVE NEUTRAL OPTION

These three-position switches control or specify the peak-to-peak signal level amplitudes of the various input and output signals that are associated with these switches on the back panel.

For the RECEIVE DATA, XMIT CLOCK IN and RECEIVE CLOCK input signals, their associated signal level switches should be set as follows:

3.6.1 POSITIVE NEUTRAL Position

For input signals that vary from 0 to +25 volts.

3.6.2 POLAR Position

For input signals that vary from ±25 volts.

3.6.3 NEGATIVE NEUTRAL Position

For input signals that vary from 0 to -25 volts.

For the XMIT DATA and XMIT CLOCK OUT output signals, their associated signal level switches should be set as follows:

3.6.4 POSITIVE NEUTRAL Position

Output signals will vary from 0 volts to either 3, 6, 9 or 12 volts depending on internal strapping.

3.6.5 POLAR Position

Output signals will vary from ±3, ±6, ±9 or ±12 volts depending on internal strapping.

3.6.6 NEGATIVE NEUTRAL Position

Output signals will vary from 0 volts to either -3, -6, -9 or -12 volts depending on internal strapping.

Internal strapping is accomplished manually on the top-most printed circuit board inside the test set. The strapping points are clearly labeled on the printed circuit board.

4.0 THEORY OF OPERATION

To test a modem or a digital communication system for proper operation, we want a test set which will produce digital data to be used as an input to the modem or system and which will be able to look at the output of the modem or system and decide whether the digital information coming out is the same as that which was put in. Further, if the modem or sys tem being tested is causing errors in the data, we want our test set to be able to tell us how many. And, finally, we want our test set to tell us that the modem or system can handle any data pattern that it might possibly see, not just one or two or three particular patterns.

Why do we use PR? Let us back up for a moment and ask ourselves what would be the best way to test a transmitter/transmission path/receiver system which is supposed to operate over a given band of frequencies and a given range of amplitudes. The answer, of course, would be to test it with "white noise". White noise, by definition, contains at random times ALL amplitudes within a given range. If we could prove that our system could handle ALL frequencies and ALL amplitudes within its specifications, we would be certain that it is capable of proper operation at ANY frequency and ANY amplitude within its specifications.

Here, however, we want to do digital testing rather than analog testing. So, we might say if we used "digital white noise" all of the remarks above would apply to testing our digital sys tem. Digital white noise, by definition, would contain all possible data patterns and any pattern would, unfortunately, occur at a completely random time. I say "unfortunately" because therein lies the problem. If a given pattern occurred at a random time, we could never know exactly when it was going to occur and therefore it would be extremely difficult to tell if the system handled it without error.

So, we turn our attention from a random data pattern to the next best thing. A PSEUDO RANDOM data pattern. What are the differences? In a random data pattern we would see every possible combination of "n" bits. In a PR pattern, we will see every possible combina tion of "n" bits except one. Therefore, we can say that for "n" bits, PR is almost as good as random. And, as "n" increases, PR gets closer and closer to becoming statistically equal to random. Secondly, and here is the clincher that sways us into using PR rather than random, the sequence of data patterns in a PR word is exactly, mathematically predictable and there fore is exactly repeatable.

It suddenly becomes clear that if we can generate an ALMOST random digital sequence to put into a system to be tested and then we can generate that exact same ALMOST random digital sequence to compare with the output of the system being tested, we can quite easily tell if the system being tested caused any errors in the data. AND THAT IS EXACTLY WHAT WE SAID WE WANTED OUR MODEM TEST SET TO DO.

1. We can generate a digital sequence which has a whole lot of different data patterns in it.

2. We can put this sequence into the input of the system we wish to test.

3. We can look at the output of the system being tested and tell whether it caused any errors in the data that was put into it.

We have said that PR data is easy to generate and that in a PR sequence we will see all but one of the possible patterns of "n" bits that we would expect to see in a comparable random sequence. Let us try to prove these statements through the following examples.

Two basic digital circuits form the heart of a PR generator; a shift register and an exclusive OR (sometimes called a mod 2 adder).

SHIFT REGISTER – A basic shift register is composed of two or more flip-flops. Each flip-flop is capable of storing a single bit of data. Therefore, the number of flip-flops in the register determines the number of bits it can store. Figure 5A below is a simplified logic diagram for a basic three-stage shift register.

If through the set and clear inputs, we place each flip-flop in a specific state, they will retain this data until a clock pulse is applied. At the time a clock pulse is applied, the data stored in each stage will shift one position to the right. This shift reoccurs each time a clock pulse is applied until the data stored in each of the flip-flops has appeared at the output in serial word format.

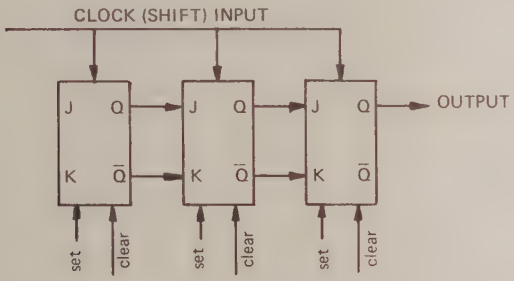
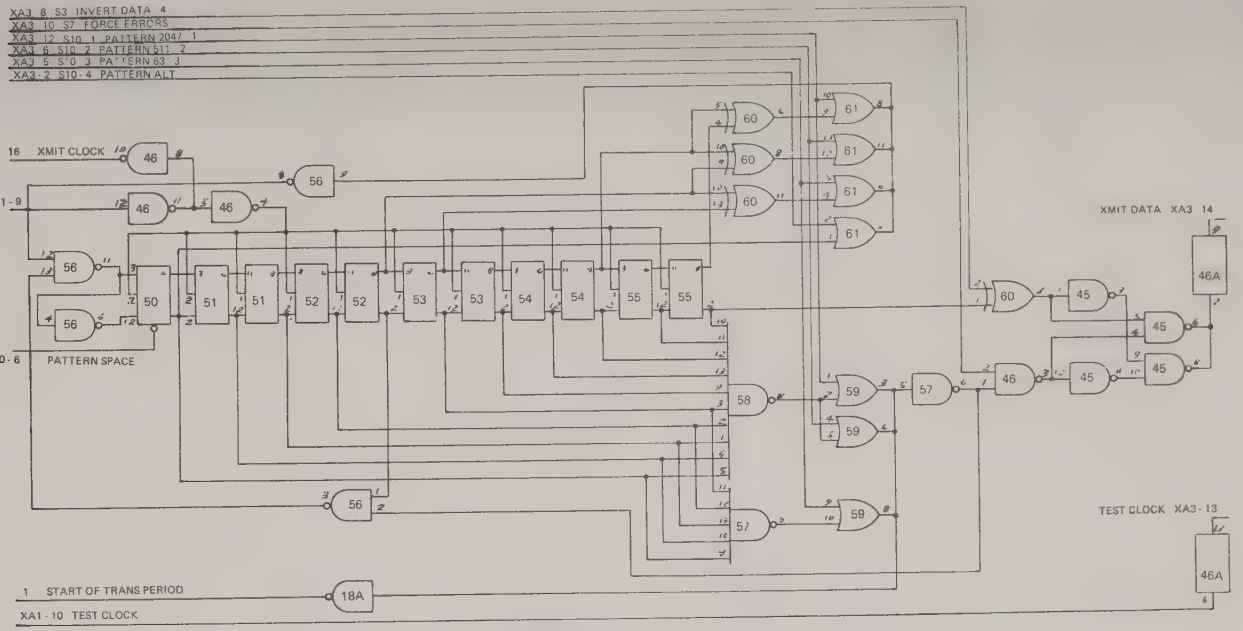
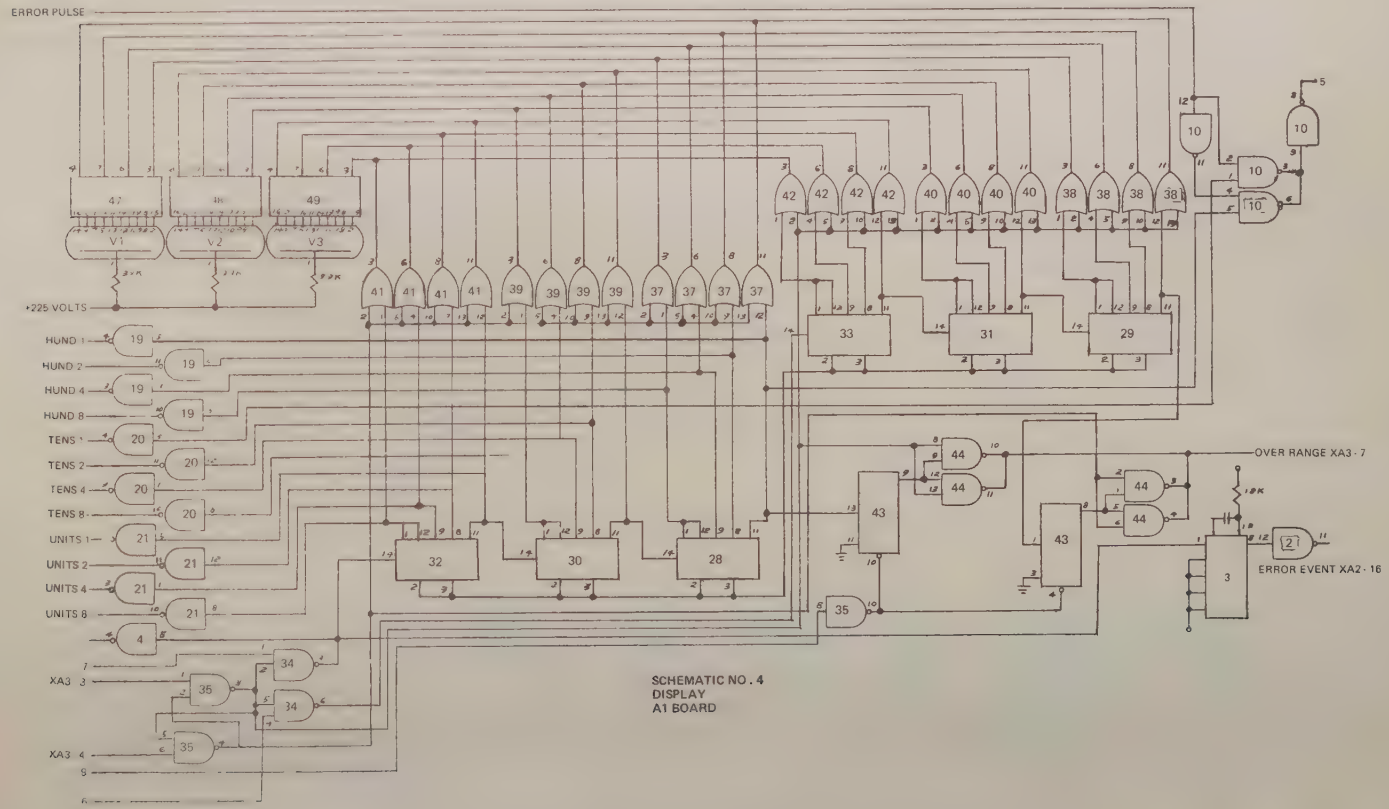


FIGURE 5A. BASIC THREE-STAGE SHIFT REGISTER



SCHEMATIC NO. 2
TRANSMITTER LOGIC
A1 BOARD



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DISPLAY
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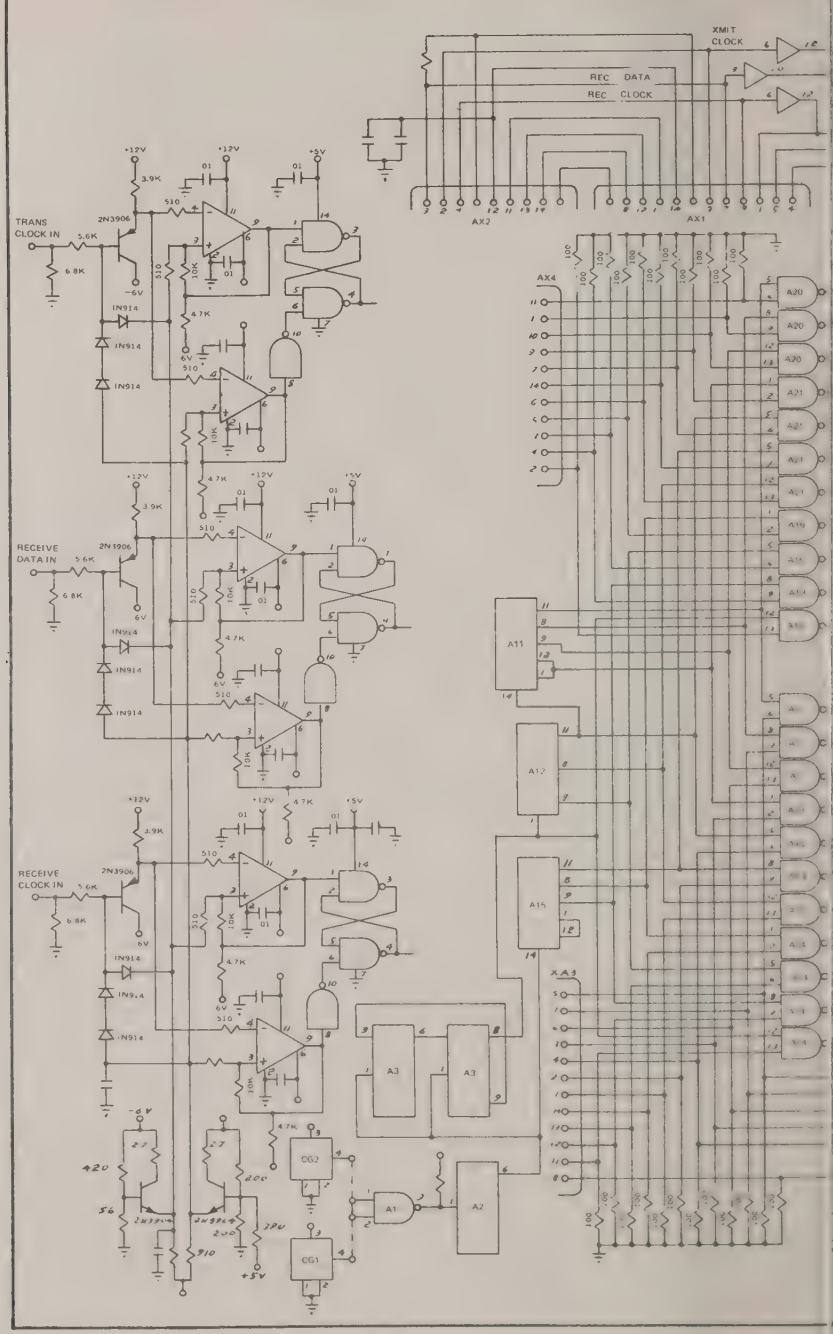
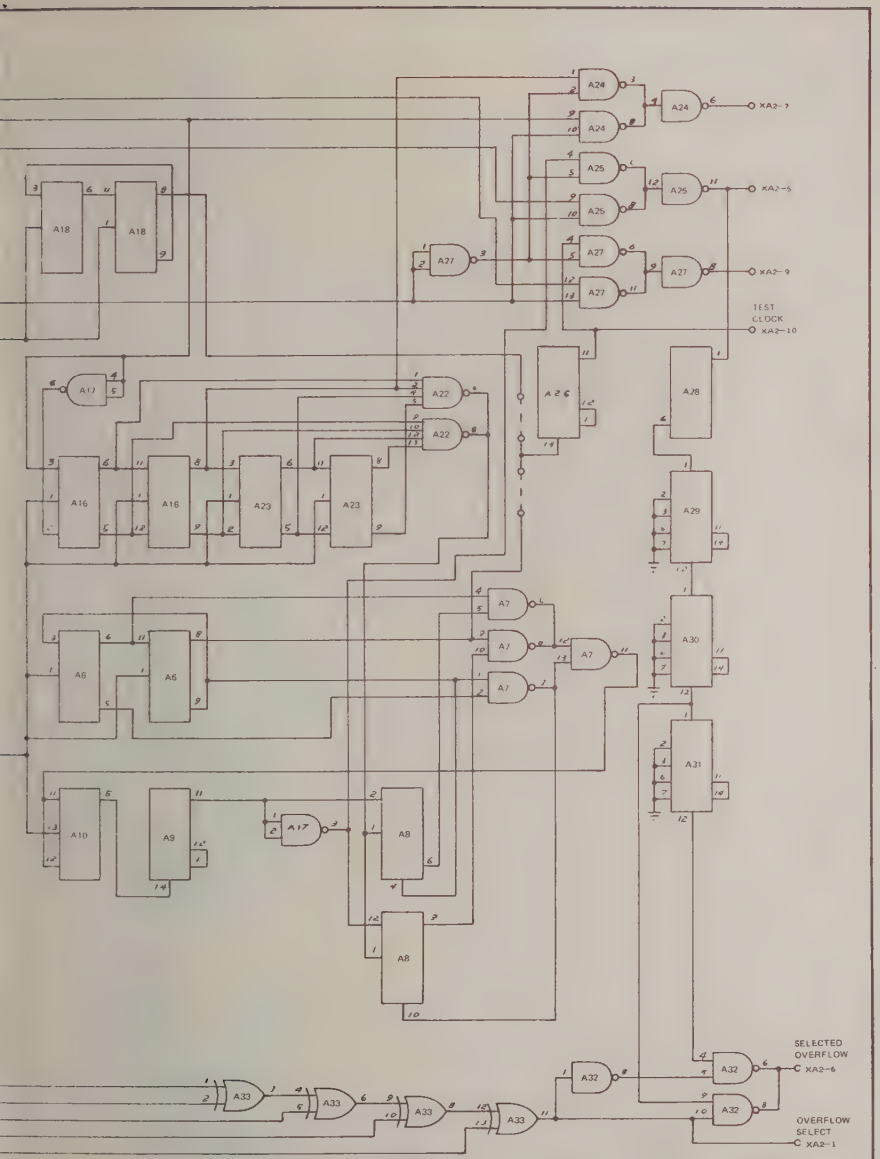

XMIT CLOCK
REC DATA
REC CLOCK
AX2
AX1
AX4
AX3
TRANS CLOCK IN
RECEIVE DATA IN
RECEIVE CLOCK IN
2N3906
IN914
A11
A12
A15
A3
A2
A1
CG2
CG1
+12V
+5V
-6V



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APPROVED			DWG C SIZE
APPROVED			
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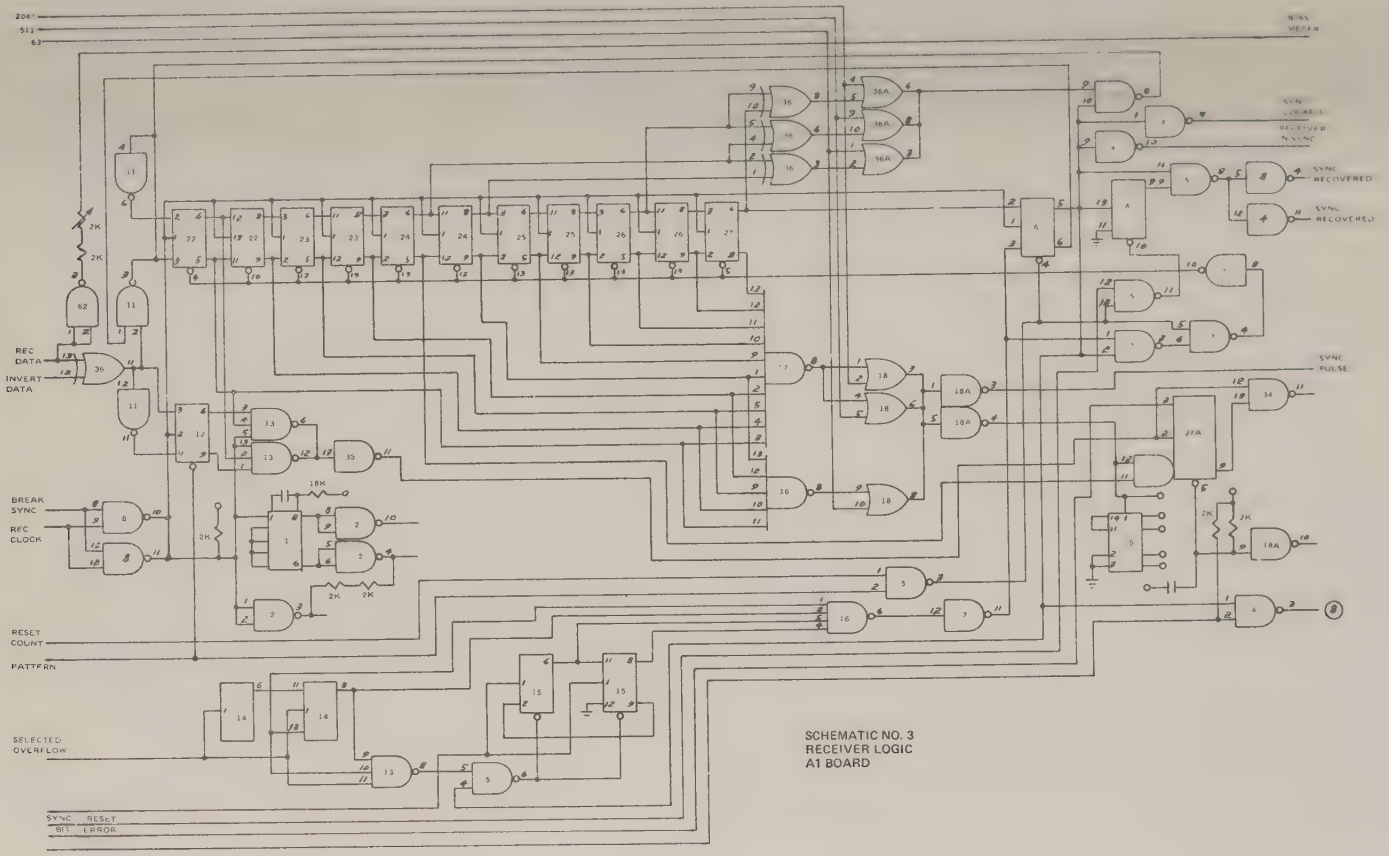

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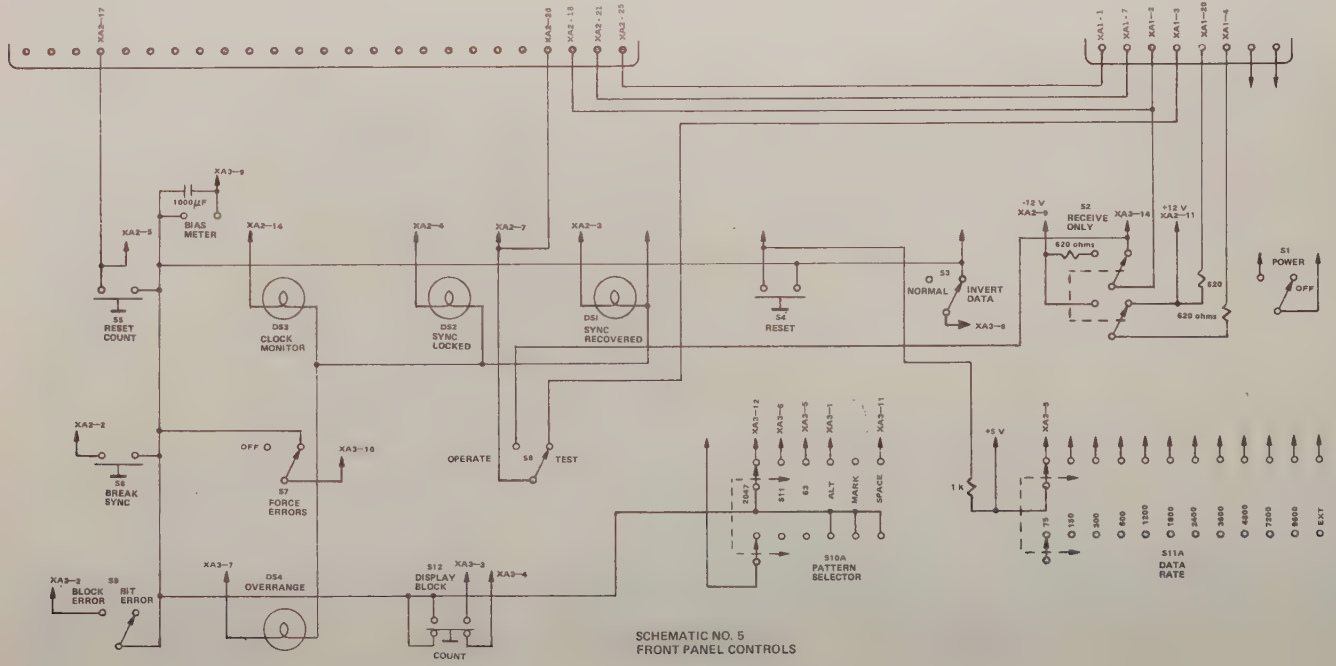
RECEIVER LOGIC
A1 BOARD



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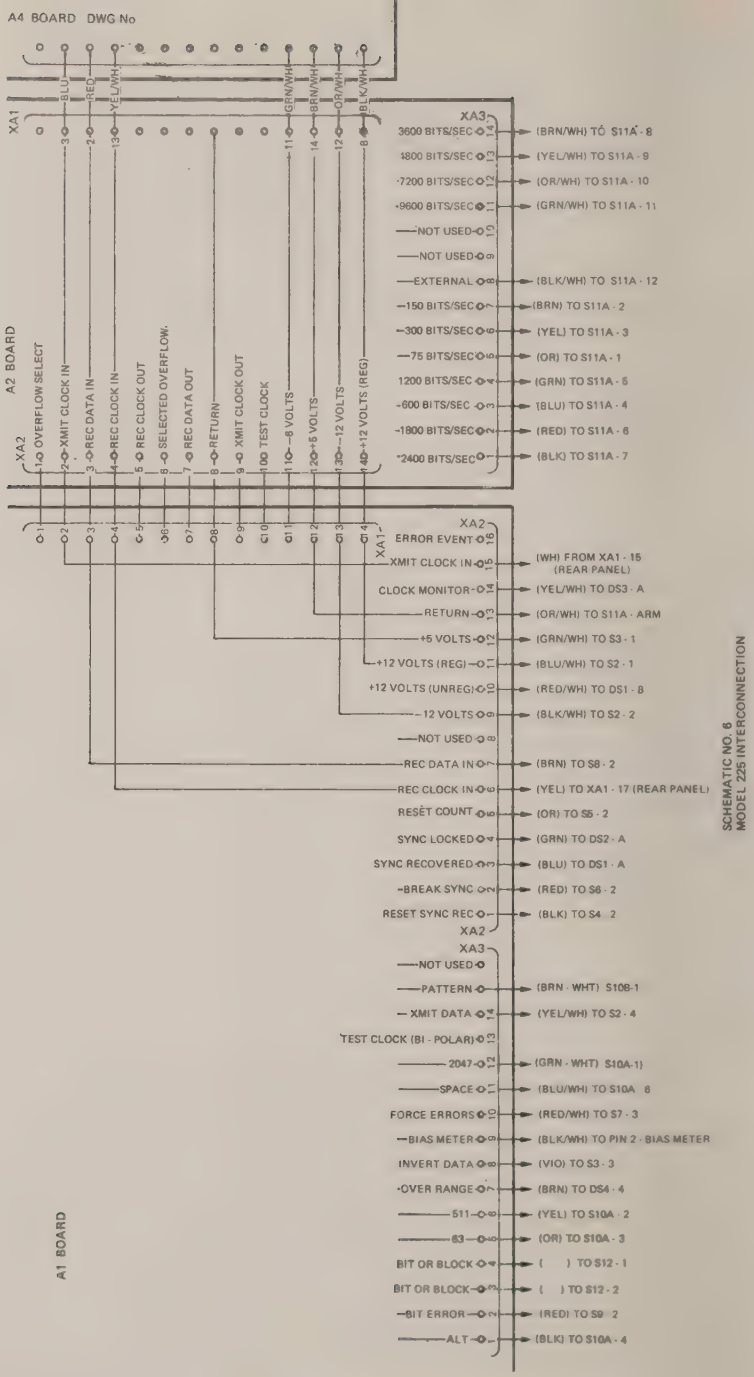
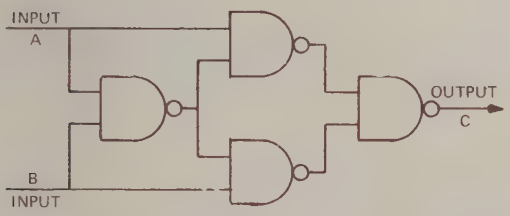
FRONT PANEL CONTROLS



SCHEMATIC NO. 6
MODEL 225 INTERCONNECTION

EXCLUSIVE OR – An exclusive OR circuit receives data at two inputs and produces one output. Figure 5B below shows the logic diagram and truth table for an exclusive OR circuit.



INPUTS		OUTPUT
A	B	C
1	1	0
0	0	0
1	0	1
0	1	1

FIGURE 5B. EXCLUSIVE OR CIRCUIT and TRUTH TABLE

From the truth table we see that if the two inputs are the same (both 1's or both 0's), the output will be a 0. If the inputs are different (a 0 and a 1 or a 1 and a 0), the output will be a 1.

Now, let us connect a basic shift register and an exclusive OR circuit as shown in Figure 5C below and see what happens.

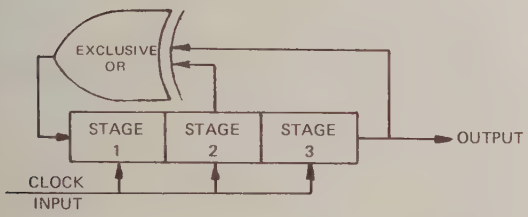


FIGURE 5C. THREE-STAGE PR GENERATOR

Let us start with stages 1, 2 and 3 having a 1, a 0 and a 0 stored in them, respectively. As we apply successive clock pulses, the following will occur simultaneously. The data stored in stages 2 and 3 are exclusively OR'd to produce an input to stage 1. The data stored in stage 1 is shifted to stage 2, that stored in stage 2 is shifted to stage 3 and that stored in stage 3 is shifted out the output. Figure 5D below shows the sequence of data in each stage of the three-stage shift register. Note that the data in each stage is exactly identical to that in each other stage but is delayed one bit time in successive stages. We see that the output (in this example taken from stage 3) is a repetitive 7 bit PR block or word.

Now let us examine the 7 bit PR word we have generated and satisfy ourselves that it does indeed contain all of the possible patterns of "n" bits except one. In our example we are using a three-stage shift register which we said is capable of storing 3 bits of information at one time. Therefore, we expect our PR sequence to contain all possible combinations of 3 bits except one. Let us examine it.

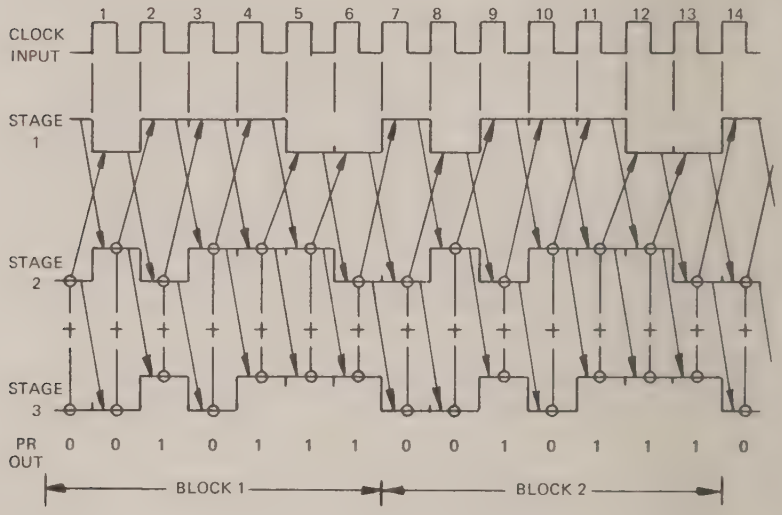


FIGURE 5D. PR WORD GENERATION USING a THREE-STAGE SHIFT REGISTER

The word we generated repetitively was "0 0 1 0 1 1 1". Using this word and a table showing all of the possible combinations of 3 bits, Figure 5E below shows that the sequence does contain all of the possible combinations except one.

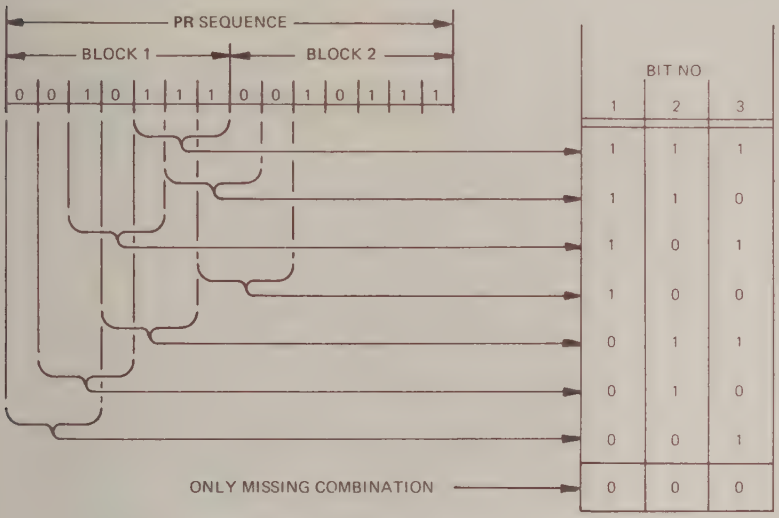


FIGURE 5E. BIT COMBINATIONS in a PR SEQUENCE

The only possible combination of 3 bits that does not occur in a PR sequence generated by a three-stage shift register is three consecutive 0's. Every other possible combination occurs once and only once in each block of the sequence.

We can show by the same analysis that a four-stage shift register will produce a repetitive PR sequence of 15 bits per block which contains all of the 16 possible combinations of 4 bits except 4 consecutive 0's; a five-stage register, 31 bits per block with all of 32 combinations except 5 consecutive 0's, etc., etc.

In general, an "n" stage shift register with exclusive OR feedback will produce a maximal length repetitive PR sequence, 2^n-1 bits in length, which contains all of the 2^n possible combinations of "n" bits except "n" consecutive 0's.

We have seen how PR data sequences are generated and have reviewed some of its properties We now have the necessary background to study how these techniques are used in the DATA-PULSE line of modem test equipment.

4.1 THE TRANSMITTER SECTION

The transmitter section of your modem test set contains the shift register and exclusive OR circuit to generate a PR sequence to be used in testing modems or digital communication systems. In addition, it also contains the circuitry for supplying clock or shift pulses to the shift register and output buffer circuitry for presenting the PR data at the output in the proper format.

a. At threaded standoff end of handle arm, add one spacer.

b. Insert this end into chassis.

c. Fasten flat washer, lock washer and lock nut to standoff. NOTE: Do not tighten lock nut completely at this time.

d. Repeat above procedure for other handle arm.

e. Locate hex handle bar between arms and fasten with No. 6–32 Phillips head screw.

f. Tighten two lock nuts located inside chassis at this time. IMPORTANT: Do not over-tighten or handle arm will not move freely.

3.4 INCREASED OPERATING SPEED OPTION

The Model 225 Modem Test Set can be optionally conditioned to operate at synchronous data rates of up to 3 MHz typical, 4 MHz maximum. The signals are made available at the rear panel utilizing four BNC connectors as shown in Figure 3 below.

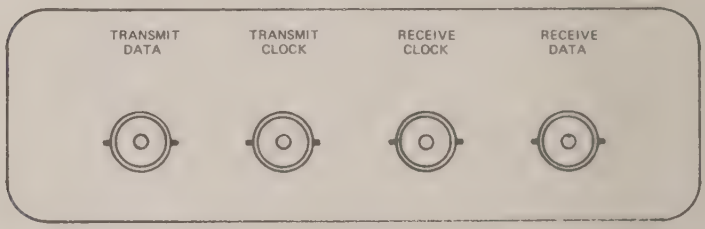


FIGURE 3. HIGH FREQUENCY SIGNALS AT REAR PANEL BNC CONNECTORS

TRANSMIT DATA is an output signal. RECEIVE DATA, RECEIVE CLOCK and TRANSMIT CLOCK are input signals. All signals are DTL TTL levels, 0 volts to +5 volts nominal. When the BNC inputs and outputs are being used, the EIA connector labeled DATA must be open. When the EIA connector inputs and outputs are being used, the BNC connectors must be open.

Let us study what happens when a data stream arrives from a system under test. The DATA SYNC switch is in position A. Let us call the first bit in the data stream BIT A (note that this was the first bit out of the transmitter PR generator), the second bit BIT B, the third BIT C, the eleventh BIT K, the twelvth BIT L, etc. BITS A through K will step into the register with the first 11 clock pulses. Let us stop the action here and examine what we have.

BIT A is in stage 11 of the receiver PR generator, BIT B in stage 10, BIT K in stage 1. The receiver PR generator now contains the identical eleven bits that were stored in the transmitter PR generator when it started sending a signal through the system being tested. The next bit that the transmitter sent was BIT L. If, at the time BIT A arrives in receiver shift register stage 11 (BIT K in stage 1), we electronically throw the DATA SYNC switch to position B, the receiver shift register will start generating a PR data stream identical to that generated by the transmitter. The next bit into stage 1 will be BIT L. This is the same as the BIT L that is coming into the receiver from the system under test. THE RECEIVER PR GENERATOR IS SYNCHRONIZED TO THE INCOMING DATA. The incoming data (if there are no errors in it) will be identical to the data being generated in the receiver PR generator at the input to stage 1 of the shift register.

Now, let us look at error detection. We learned earlier that if the two inputs to an exclusive OR circuit are the same (00 or 11), the output will be 0. If they are different (01 or 10), the output will be 1. Look again at Figure 5G above. When the DATA SYNC switch was in position A, the error detecting exclusive OR circuit was receiving the incoming data at both of its inputs simultaneously. The output of it had to be 0. After switching to position B, one of its inputs is the PR data being generated in the receiver PR generator. The other input is still the incoming data. As long as there are no errors in the incoming data, the output of the error detecting exclusive OR will be 0. If, however, the system under test has caused an error in the incoming data, the data streams, at the time of the error, will be different and the output of the exclusive OR will be 1.

We now have an instrument which:

1. Generates a PR data stream and transmits it through a system under test.

2. Synchronizes to the data stream coming from the system under test and generates a second, identical PR data stream.

3. An exclusive OR which compares the two and produces a 1 output each time there is an error in the data coming from the system being tested.

4.3 SYNCHRONIZATION

We saw above how the modem test set receiver synchronizes to the incoming data by shifting the first 11 bits of incoming data into its shift register, at which time it automatically switches to a PR generator configuration and generates a PR data stream which is started with that particular 11 bits.

Suppose though, that the system under test had caused one or more errors in the first incoming eleven bits. The receiver PR generator would then be synchronized to a false pattern and the transmitter and receiver PR generators would not really be synchronized. Many false errors would be produced from the error detecting exclusive OR. In other words, the error rate would be extremely high.

Built into the DATAPULSE Modem Test Set receivers is circuitry which constantly monitors the error output. If it detects error rates above a certain preset figure, it automatically switches the DATA SYNC switch back to position A and goes through the entire synchronization cycle again. It will continue to do this automatically until it does synchronize on valid data.

4.4 CLOCK CORRECTION

When testing synchronous modems or synchronous systems, a clock which is synchronized with the data is supplied by the modem to the test set receiver. When testing asynchronous systems however, a clock for the test set receiver section must be generated within the test set. Basically, the clock for both the transmitter and receiver portions of the DATAPULSE test sets are derived from a crystal controlled oscillator divided down to the desired data rate. What though if there are delays through the system being tested that vary from time to time, having the effect of varying the clock time of the transmitted data with respect to the clock time of the receiver generated data. This would have the effect of de-synchronizing the two data streams and errors would be sensed even though there might not be any in the in coming data.

In order to eliminate this possibility, DATAPULSE Modem Test Sets contain circuitry which automatically and continuously corrects the receiver clock frequency so that the receiver clocks are always very nearly coincident in time with transition times of the incoming data. Figure 5H below is a simplified block and timing diagram of this clock correction circuit.

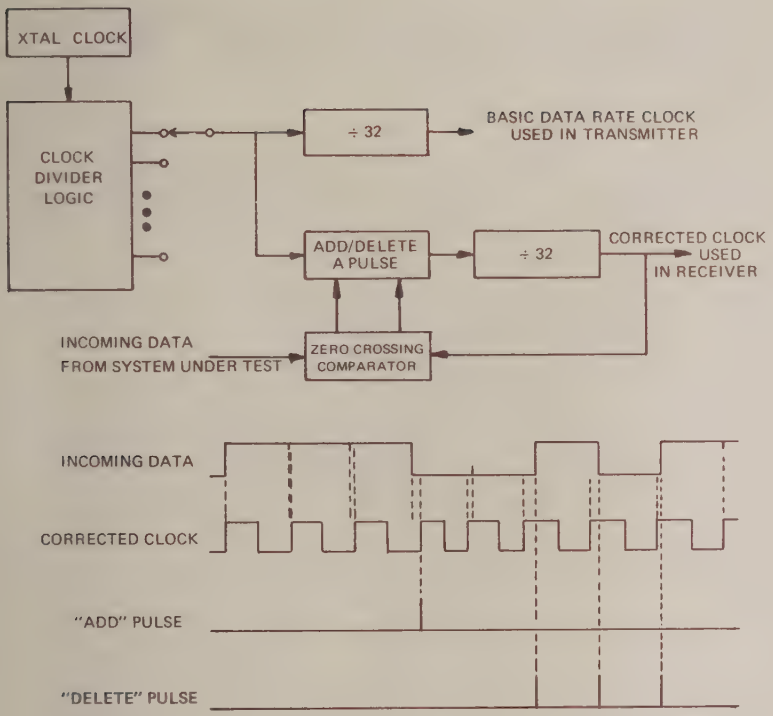


FIGURE 5H. BLOCK and TIMING DIAGRAM—CLOCK CORRECTION CIRCUIT

A basic frequency is selected in the receiver which is 32 times the frequency of the basic data rate being used in the transmitter. This signal is put through a "Add/Delete a Pulse" circuit and is then divided by 32 to form the clock to be used in the receiver. If there was no instruction to add or delete a pulse, the frequency of the receiver clock is the same as that of the transmitter clock and the transitions of the incoming data coincide with the clock times of the receiver.

If however, for any reason the transition time of an incoming data bit occurs prior to the positive-going edge of a receiver clock, the Zero Crossing Comparator will detect this and will add one pulse to the 32 times data rate stream. When this stream is subsequently divided by 32, the corrected clock output will occur slightly sooner than normal and the receiver clock will be corrected in the proper direction to make it coincide with the incoming data transition times. If, on the other hand the clock starts to occur before the data transition time, a pulse will be delected from the 32 times data rate stream and the corrected clock will be corrected in the opposite direction.

The clock correction circuitry will continuously make comparisons with each transition of the incoming data and correct the receiver clock so that it is timed coincident with the incoming data.

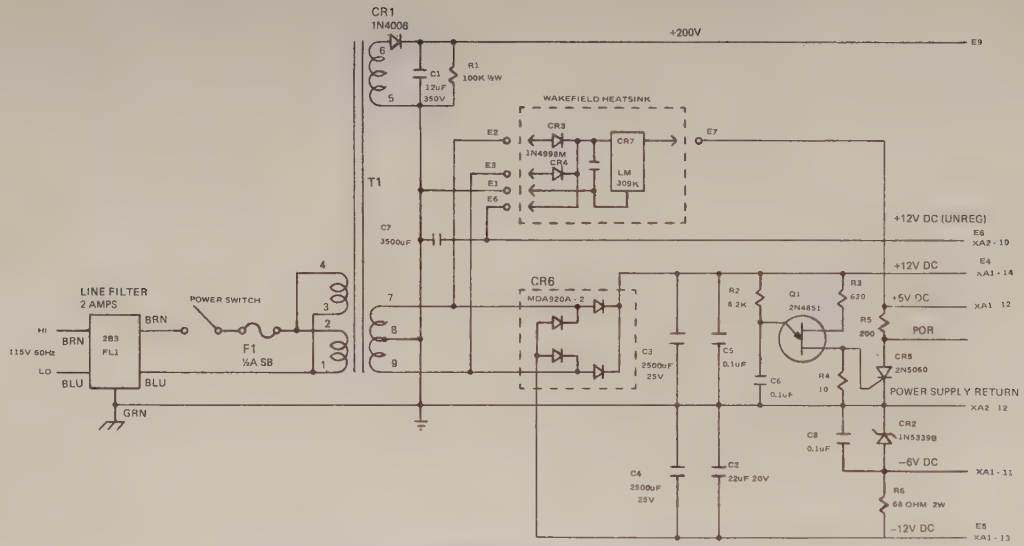
4.5 BIT/BLOCK ERROR COUNT AND DISPLAY

The receiver portion of each DATAPULSE Modem Test Set contains counter circuitry for counting either each bit that is in error or each block which contains one or more errors. On some models only bit errors may be counted. On others bit or block error count may be selected by front panel switch.

The output of this counter is continuously displayed on a three-digit nixie display at the instrument front panel. A front panel overrange indicator lights when the count on the error indicator passes through a count of 999. Thus, a total error count of 1,999 may be displayed without resetting the counter.

4.6 BLOCK COUNT

One modem test set contains a second counter which continuously counts blocks of data received regardless of errors. This counter may be displayed on the bit/block error display by actuation of a front panel pushbutton.



SCHEMATIC NO. 7
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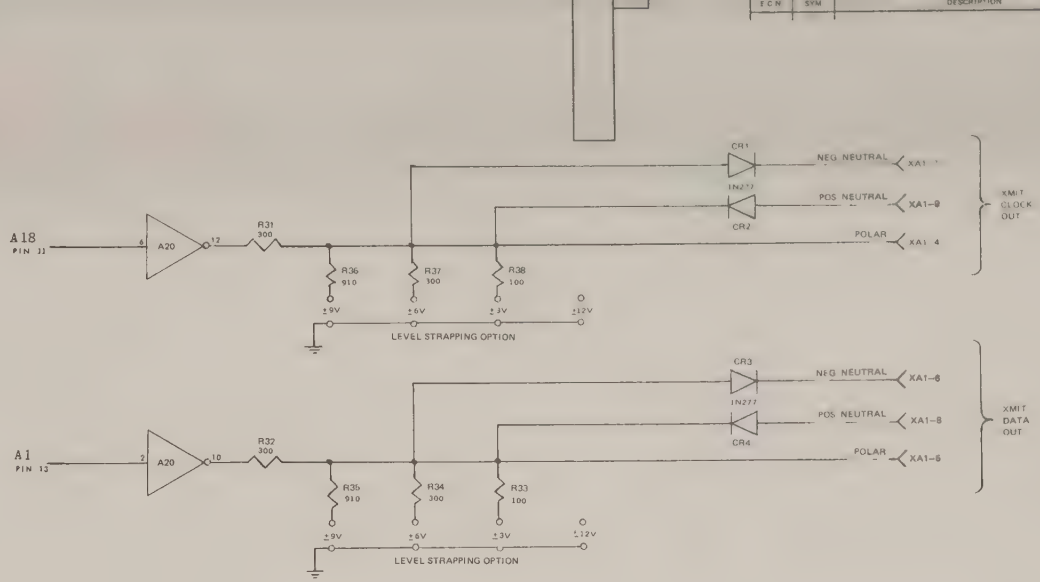

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±	±	±
MATERIAL		
FINISH		
DO NOT SCALE DWG.		

DRAWN	
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APPROVED	
RELEASED	

TITLE

SCHEMATIC NO. 8
NEGATIVE NEUTRAL, POLAR AND
POSITIVE NEUTRAL OPTION

DATAPULSE
DATAPULSE, INC.
CULVER CITY, CALIFORNIA

DWG	
B	
SIZE	

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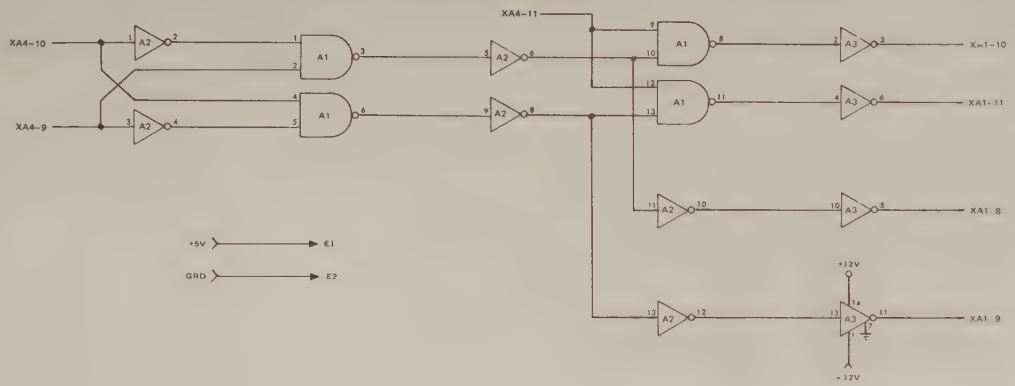

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			APPROVED			
FINISH			APPROVED			DWG B SIZE
DO NOT SCALE DWG.			RELEASED		SCALE	CODE 15933 SHEET OF

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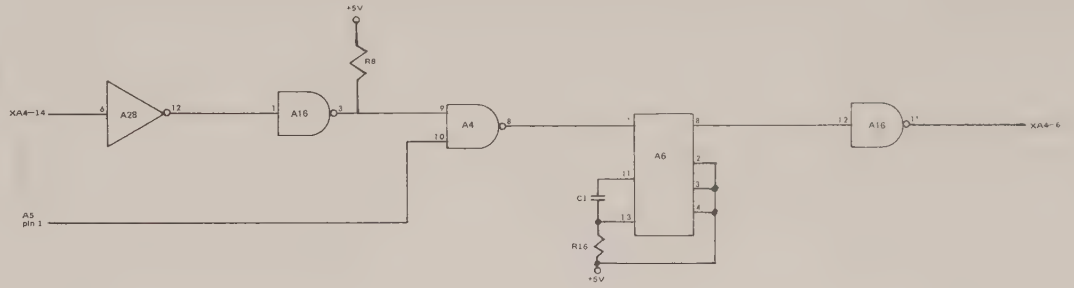

NOTES: UNLESS OTHERWISE SPECIFIED

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APPLICATION		QTY REQD	

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TOLERANCES ON
3 PLACE DEC. ± | 2 PLACE DEC. ± | ANGLES ±
MATERIAL
FINISH
DO NOT SCALE DWG.

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TITLE
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SCALE
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DATAPULSE
DATAPULSE, INC.
CULVER CITY, CALIFORNIA

SIZE B
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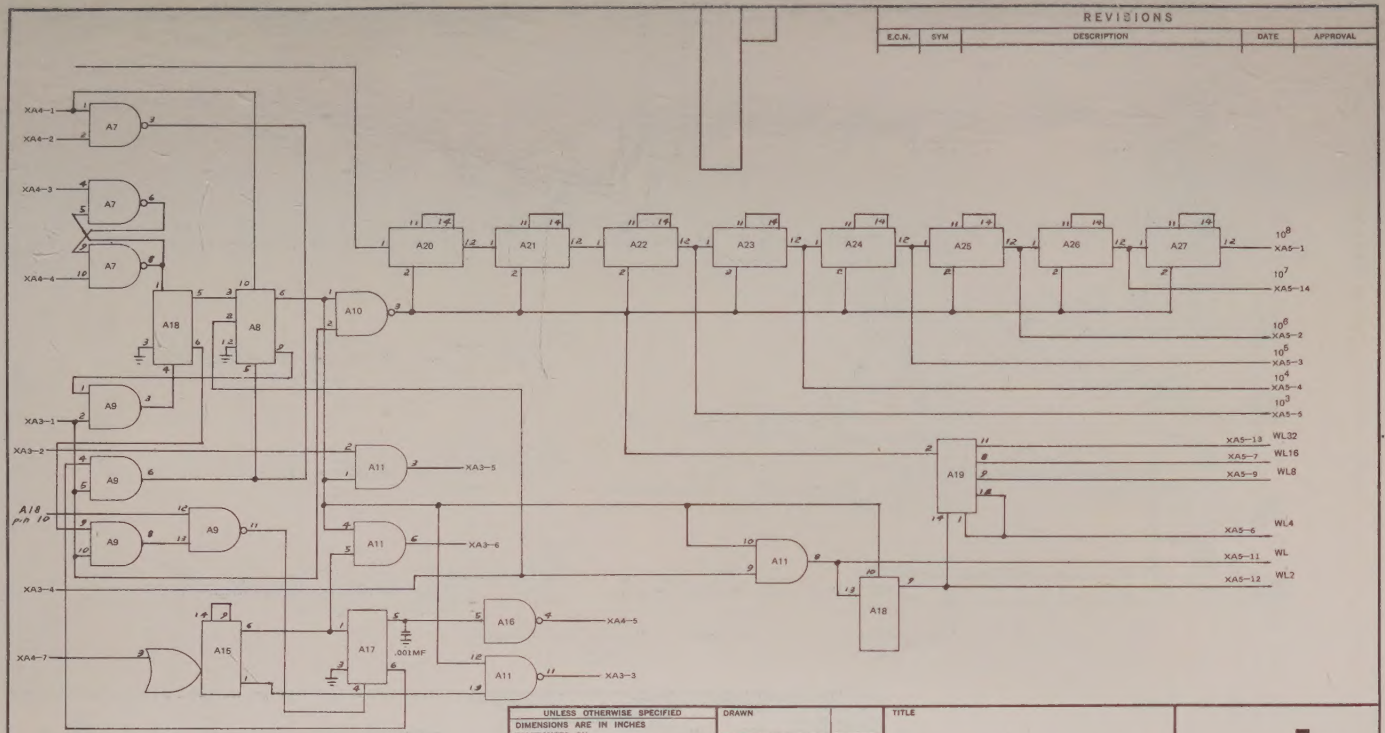
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DATAPULSE
DATAPULSE, INC.
CULVER CITY, CALIFORNIA
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OF
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APPLICATION | QTY REQD
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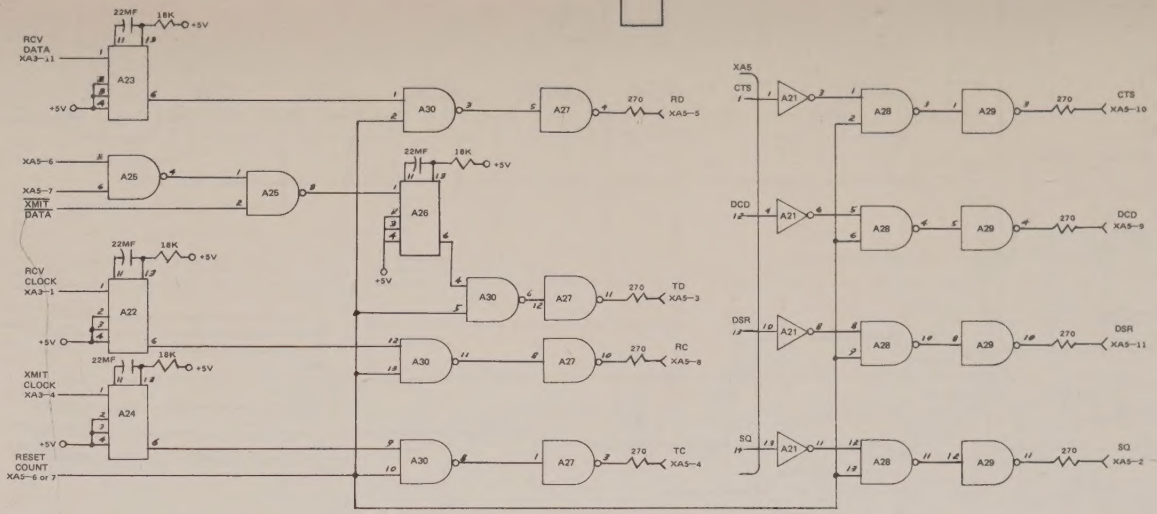

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MATERIAL			APPROVED	
FINISH			APPROVED	
DO NOT SCALE DWG.			RELEASED	

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APPLICATION		QTY REQD	

TITLE: SCHEMATIC NO. 12
MONITOR LIGHTS OPTION

SCALE | CODE 15933

DATAPULSE, INC.
CULVER CITY, CALIFORNIA

DWG B SIZE

SHEET OF

MP MASTER
MA28867

SYSTRON-DONNER CORPORATION
DATAPULSE